Claims:
This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (previously presented)

An integrated circuit testing apparatus, comprising:

a test circuit operable to produce a signal for determining at least one of an operating reference signal and a substrate coupling effect on a plurality of components within an integrated circuit, said test circuit having a ring oscillator which mimics a data path within said integrated circuit, wherein said ring oscillator is powered by an external power supply; and

a test circuit operable to produce a signal for determining at least one of a cross-talk effect on said plurality of components and the accuracy of an interconnect capacitance extraction value.

Claim 2 (previously presented)

An integrated circuit testing apparatus, comprising:

a test circuit operable to produce a signal for determining at least one of an operating reference signal and a substrate coupling effect on a plurality of components within an integrated circuit, said test circuit having a ring oscillator which mimics a data path within said integrated circuit, wherein said ring oscillator is powered by an external power supply; and

a test circuit operable to produce a signal for determining at least one of an effect of system noise on the operational speed of said plurality of components and a maximum degradation expected for a logic path between said plurality of components.

Claim 3 (currently amended)

An integrated circuit testing apparatus, comprising:

a test circuit operable to produce a signal for determining at least one of an operating reference signal and a substrate coupling effect on a plurality of components within an integrated circuit; and

a test circuit operable to produce a signal for determining an effect of power supply noise on a signal propagation delay within said plurality of components;

wherein said test circuit operable to produce a signal for determining an effect of power supply noise on a signal propagation delay within said plurality of components within said

integrated circuit includes a ring oscillator which mimics a data path within said integrated circuit, wherein said ring oscillator shares a power supply with a core logic area of said integrated circuit.

Claim 4 (previously presented)

An integrated circuit testing apparatus, comprising:

a test circuit operable to produce a signal for determining at least one of a cross-talk effect on a plurality of components within an integrated circuit and the accuracy of an interconnect capacitance extraction value, said test circuit having a ring oscillator routed within a core logic area of said integrated circuit, wherein said ring oscillator is powered by an external power supply; and

a test circuit operable to produce a signal for determining at least one of an effect of system noise on the operational speed of said plurality of components and a maximum degradation expected for a logic path between said plurality of components.

Claim 5 (currently amended)

An integrated circuit testing apparatus, comprising:

a test circuit operable to produce a signal for determining at least one of a cross-talk effect on a plurality of components within an integrated circuit and the accuracy of an interconnect capacitance extraction value; and

a test circuit operable to produce a signal for determining an effect of power supply noise on a signal propagation delay within said plurality of components;

wherein said test circuit operable to produce a signal for determining at least one of a cross-talk effect on said plurality of components within said integrated circuit and the accuracy of an interconnect capacitance extraction value includes a ring oscillator routed within a core logic area of said integrated circuit, wherein said ring oscillator is powered by an external power supply.

Claim 6 (currently amended)

An integrated circuit testing apparatus, comprising:

a test circuit operable to produce a signal for determining at least one of an effect of system noise on the operational speed of a plurality of components within an integrated circuit and a maximum degradation expected for a logic path between said plurality of components; and

a test circuit operable to produce a signal for determining an effect of power supply noise on a signal propagation delay within said plurality of components;

wherein said test circuit operable to produce a signal for determining at least one of an effect of system noise on the operational speed of said plurality of components within said integrated circuit and a maximum degradation expected for a logic path between said plurality of components includes a ring oscillator randomly located within a core logic area of said integrated circuit, wherein said ring oscillator is powered by an external power supply.

Claim 7 (canceled)

Claim 8 (currently amended)

The apparatus of ~~claims 1 or 5~~ claim 1 wherein said test circuit operable to produce a signal for determining at least one of a cross-talk effect on said plurality of components within said integrated circuit and the accuracy of an interconnect capacitance extraction value includes a ring oscillator routed within a core logic area of said integrated circuit, wherein said ring oscillator is powered by an external power supply.

Claim 9 (currently amended)

The apparatus of ~~claims 2 or 6~~ claim 2 wherein said test circuit operable to produce a signal for determining at least one of an effect of system noise on the operational speed of said plurality of components within said integrated circuit and a maximum degradation expected for a logic path between said plurality of components includes a ring oscillator randomly located within a core logic area of said integrated circuit, wherein said ring oscillator is powered by an external power supply.

Claim 10 (currently amended)

The apparatus of ~~claims 3 or 6~~ claim 6 wherein said test circuit operable to produce a signal for determining an effect of power supply noise on a signal propagation delay within said plurality of components within said integrated circuit includes a ring oscillator which mimics a data path within said integrated circuit, wherein said ring oscillator shares a power supply with a core logic area of said integrated circuit.